

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended): A data processing device using pipeline control, comprising:

an instruction queue in which a plurality of instruction codes are fetched and stored;

a fetch address operation circuit ~~[[which]]~~ that calculates a fetch address, the fetch address being used to fetch and store an instruction code in the instruction queue;

a fetch circuit ~~[[which]]~~ that fetches an instruction code, ~~that is the~~ instruction code being read out from a memory based on the fetch address and being stored into the instruction queue; and

a branch information setting circuit ~~[[which]]~~ that decodes a branch setting instruction, ~~wherein the branch setting instruction explicitly or implicitly specifies~~ specifying a branch occurring address and a branch target address, ~~wherein a branch to the branch target address occurs~~ occurring when the fetch address is the branch occurring address after a x-th instruction from the branch setting instruction, the branch information setting circuit stores storing the branch occurring address in a branch occurring address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded,

~~wherein the fetch address operation circuit includes~~ including a circuit ~~[[which]]~~ that compares one of a previous fetch address and an expected next fetch address with a value stored in the branch occurring address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address, based on the comparison result.

2. (Currently Amended): A data processing device using pipeline control, comprising:

an instruction queue in which a plurality of instruction codes are fetched and stored;

a fetch address operation circuit ~~[[which]]~~ that calculates a fetch address, the fetch address being used to fetch and store an instruction code in the instruction queue;

a fetch circuit ~~[[which]]~~ that fetches an instruction code, that is the instruction code being read out from a memory based on the fetch address and being stored into the instruction queue; and

a branch information setting circuit ~~[[which]]~~ that decodes a branch setting instruction, ~~wherein~~ the branch setting instruction explicitly or implicitly specifies specifying a branch occurring address and a branch target address, ~~wherein~~ a branch to the branch target address ~~occurs~~ occurring when the fetch address is the branch occurring address after a x-th instruction from the branch setting instruction, the branch information setting circuit stores storing the branch occurring address in a branch occurring address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded,

~~wherein~~ the fetch address operation circuit ~~includes~~ including a circuit ~~[[which]]~~ that compares an expected next fetch address obtained by incrementing a value in a fetch program counter by one instruction length with a value stored in the branch occurring address storage register, and then outputs a value stored in the branch target address storage register as a next fetch address when the expected next fetch address coincides with the value in the branch occurring address storage register, or outputs the expected next fetch address as a next fetch address when the expected next fetch address does not coincide with the value in the branch occurring address storage register.

3. (Currently Amended): The data processing device as defined in claim 1, wherein:

the branch setting instruction ~~includes~~ including a loop instruction ~~[[which]]~~ that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit ~~decodes~~ decoding the loop instruction ~~which instructs to repeat a branch to the branch target address the number of times equal to the loop count,~~ and stores storing the loop count designated by the loop instruction; and

the fetch address operation circuit ~~includes~~ including a circuit ~~[[which]]~~ that outputs a value that is stored in the branch target address storage register as a next fetch address until the number of times the branch to the branch target address ~~occurs~~repeats reaches the loop count.

4. (Currently Amended): The data processing device as defined in claim 2, wherein:

the branch setting instruction ~~includes~~ including a loop instruction ~~[[which]]~~ that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit ~~decodes~~ decoding the loop instruction ~~which instructs to repeat a branch to the branch target address the number of times equal to the loop count,~~ and stores storing the loop count designated by the loop instruction; and

the fetch address operation circuit ~~includes~~ including a circuit ~~[[which]]~~ that outputs a value that is stored in the branch target address storage register as a next fetch address until the number of times the branch to the branch target address ~~occurs~~repeats reaches the loop count.

5. (Currently Amended): The data processing device as defined in claim 1, wherein:

the branch setting instruction ~~includes~~ including a loop instruction ~~[[which]]~~ that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit ~~decodes~~ decoding the loop instruction ~~which instructs to repeat a branch to the branch target address the number of times equal to the loop count,~~ and stores storing the loop count designated by the loop instruction into a loop counter; and

the fetch address operation circuit ~~includes~~ including a circuit ~~[[which]]~~ that decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value that is obtained by incrementing the branch occurring address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

6. (Currently Amended): The data processing device as defined in claim 2, wherein:

the branch setting instruction ~~includes~~ including a loop instruction ~~[[which]]~~ that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit ~~decodes~~ decoding the loop instruction ~~which instructs to repeat a branch to the branch target address the number of times equal to the loop count,~~ and stores storing the loop count designated by the loop instruction into a loop counter; and

the fetch address operation circuit ~~includes~~ including a circuit ~~[[which]]~~ that decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value that is obtained by incrementing the branch occurring address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

7. (Currently Amended): The data processing device as defined in claim 3[[.]] wherein:

the branch setting instruction ~~includes~~ including a loop instruction [[which]] that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit ~~decodes~~ decoding the loop instruction ~~which instructs to repeat a branch to the branch target address the number of times equal to the loop count,~~ and ~~stores~~ storing the loop count designated by the loop instruction into a loop counter; and

the fetch address operation circuit ~~includes~~ including a circuit [[which]] that decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value that is obtained by incrementing the branch occurring address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

8. (Currently Amended): The data processing device as defined in claim 4, wherein:

the branch setting instruction ~~includes~~ including a loop instruction [[which]] that designates a loop count and instructs to repeat a branch from the branch occurring address to the branch target address the number of times equal to the loop count;

the branch information setting circuit ~~decodes~~ decoding the loop instruction ~~which instructs to repeat a branch to the branch target address the number of times equal to the loop count,~~ and ~~stores~~ storing the loop count designated by the loop instruction into a loop counter; and

the fetch address operation circuit ~~includes~~ including a circuit which that decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value that is obtained by incrementing the branch occurring address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

9. (Currently Amended): The data processing device as defined in claim 3[[.]] wherein:

the loop instruction ~~has the branch target address which is fixed relative to the loop instruction and also has~~ having no branch target address information in an operand; and

the branch information setting circuit ~~includes~~ including a circuit [[which]] that calculates the branch target address based on the address in memory where the loop instruction is stored and a [[the]] fixed value ~~fixed relative to the loop instruction~~ and stores the calculated value in the branch target address storage register.

10. (Currently Amended): The data processing device as defined in claim 4[[.]] wherein:

the loop instruction ~~has the branch target address which is fixed relative to the loop instruction and also has~~ having no branch target address information in an operand; and

the branch information setting circuit ~~includes~~ including a circuit [[which]] that calculates the branch target address based on the address in memory where the loop instruction is stored and a [[the]] fixed value ~~fixed relative to the loop instruction~~ and stores the calculated value in the branch target address storage register.

11. (Currently Amended): The data processing device as defined in claim 5[[.]] wherein:

the loop instruction ~~has the branch target address which is fixed relative to the loop instruction and also has~~ having no branch target address information in an operand; and

the branch information setting circuit ~~includes~~ including a circuit [[which]] that calculates the branch target address based on the address in memory where the loop instruction is stored and a [[the]] fixed value ~~fixed relative to the loop instruction~~ and stores the calculated value in the branch target address storage register.

12. (Currently Amended): The data processing device as defined in claim 6[[,]] wherein:

the loop instruction ~~has the branch target address which is fixed relative to the loop instruction and also has~~ having no branch target address information in an operand; and

the branch information setting circuit ~~includes including a circuit [[which]] that calculates the branch target address based on the address in memory where the loop instruction is stored and a [[the]] fixed value fixed relative to the loop instruction~~ and stores the calculated value in the branch target address storage register.

13. (Currently Amended): Electronic equipment comprising:
the data processing device as defined in claim 1;
means for receiving input data; and
means for outputting a result of a process performed processing the input data by the data processing device based on the input data.

14. (Currently Amended): Electronic equipment comprising:
the data processing device as defined in claim 2;
means for receiving input data; and
means for outputting a result of a process performed processing the input data by the data processing device based on the input data.

15. (Currently Amended): Electronic equipment comprising:
the data processing device as defined in claim 3;
means for receiving input data; and
means for outputting a result of a process performed processing the input
~~data~~ by the data processing device based on the input data.

16. (Currently Amended): Electronic equipment comprising:
the data processing device as defined in claim 4;
means for receiving input data; and
means for outputting a result of a process performed processing the input
~~data~~ by the data processing device based on the input data.

17. (Currently Amended): Electronic equipment comprising:
the data processing device as defined in claim 5;
means for receiving input data; and
means for outputting a result of a process performed processing the input
~~data~~ by the data processing device based on the input data.

18. (Currently Amended): Electronic equipment comprising:
the data processing device as defined in claim 6;
means for receiving input data; and
means for outputting a result of a process performed processing the input
~~data~~ by the data processing device based on the input data.